Device and Method for Temperature-Based Control over Write and/or Read Operations," U.S. patent application serial no. 09/944,413 (attorney docket no. 10519/22; MD-54), which is being filed on the same day as the present application and is hereby incorporated by reference. In addition to providing an input to the mode register 430, the same or another temperature control circuit can be used to implement the thermal cut-off techniques described in the above-referenced patent application to protect the memory array 400 from functionality failure at high temperature.

There are several alternatives that can be used with these preferred embodiments. For example, instead of using a data register partitioned into eight separate registers as in Figure 1, a single input/output data register 500 can be used, as shown in Figure 5. In this alternate embodiment, the data register 500 has eight separate register ports, each connected to a respective sub-array group via respective data busses. The register selection logic 140 of Figure 1 is replaced by port control logic 540. The number of register ports and sub-array groups that are active at one time is controlled by the value in the mode register 530. Specifically, the value in the mode register 530 determines how many sub-array groups are activated by the sub-array group selection logic 510 and also determines how many register ports in the data register 500 are activated by the port control logic 540. The operation of this alternate embodiment is similar to that of the embodiment shown in Figure 1.

In another alternate embodiment shown in Figure 6, an input/output data register 600 is connected to the controlling inputs of a variable serial-to-parallel connection circuit 605 via eight byte-wide data busses. The connection circuit 605 provides a path from the data register 600 (which can contain, for example, 512 bytes of information) to the memory array (which can contain, for example, 2^{16} more bytes of information). Each sub-array group has a byte-wide data bus connected to the connection circuit 605. The variable serial-to-parallel connection circuit 605 changes from one to eight parallel paths to the memory array. In this embodiment, the change in serial-to-parallel mapping is preferably a power of two for simplicity in logic design; however, a non-power-of-two change in mapping can be used. Preferably, the ECC bits for a write operation are

than in an air-conditioned building). Because of these unknown factors, the maximum data rate is often designed to be low enough so that both typical memory arrays and most worst-case memory arrays (*e.g.*, memory arrays with defects, poor heat transfer packaging, or high ambient temperatures) will operate below the thermal run-away temperature. Accordingly, the maximum data rate for a typical memory array is lower than required.

The assignee of the present invention has developed a technique for sensing the temperature state of a memory array and preventing a write and/or read operation to the memory array when the temperature of the memory array reaches a threshold temperature. This technique is described in "Memory Device and Method for Temperature-Based Control over Write and/or Read Operations," U.S. patent application serial no. 09/944,615 (attorney docket no. 10519/22; MD-54), which is being filed on the same day as the present application and is hereby incorporated by reference. By preventing write and/or read operations only when the memory array is too hot, this technique avoids thermal run-away in worst-case memory arrays while maintaining a high data rate in typical memory arrays. While useful in many applications, this technique can result in a relatively low data rate in applications where write and/or read operations are frequently interrupted due to high operating temperatures.

The preferred embodiments described herein provide another technique that can be used to avoid thermal run-away while maintaining a relatively high data rate. By way of overview, a memory array is provided that comprises a plurality of groups of sub-arrays. As used herein, a sub-array is a contiguous group of memory cells having contiguous word and bit lines generally unbroken by decoders, drivers, sense amplifiers, and input/output circuits. A "group" of sub-arrays can comprise a single sub-array or a plurality of sub-arrays. In these preferred embodiments, the number of sub-array groups that is simultaneously written into is selectable and can vary. For example, the memory array can have a default number of groups of sub-arrays that can be simultaneously written into, and this number can be increased (or decreased) to select a different number of sub-array groups that can be simultaneously written into. Alternatively, an input source (*e.g.*, a host device, a tester, a component in the memory device) can set the